30V N-Ch Power MOSFET

Feature

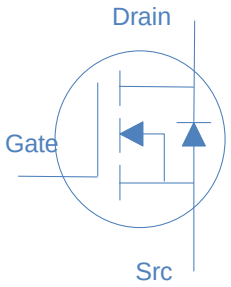
- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested 100% Rg Tested
- Lead Free, Halogen Free

DS			
DS(on),typ	GS		Ω
D (Sillicon Limited)			

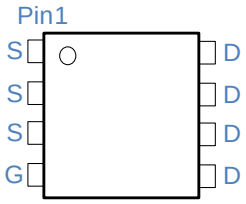
Application

- Hard Switching and High Speed Circuit
- DC/DC In Telecoms and Industrial

DFN5x6



Part Number	Package	Marking
	DFN5x6	



=25 (unless otherwise specified)

Parameter	Symbol	Conditions		
Continuous Drain Current (Silicon Limited)		=25		
		=100		
Drain to Source Voltage	DS			
Gate to Source Voltage	GS			
Pulsed Drain Current				
Avalanche Energy, Single Pulse	AS	L=0.1mH, T =25		mJ
Power Dissipation		=25		W
Operating and Storage Temperature	J, T			

Parameter	Symbol		
Thermal Resistance Junction-Ambient	θJA		/W
Thermal Resistance Junction-Case	θJC		/W

Electrical Characteristics at T =25 (unless otherwis " Ò Ï↑ at Ê ï rs

Drain to Source on Resistance		Ω
	$_{DS}$=5V, I	S
Gate Resistance	$_{GS}$=15mV, V_{DS} =0V, f=1MHz	Ω
Input Capacitance		
	$_{GS}$=0V, V_{DS}=15V, f=1MHz	pF
	rss	

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

Figure 9. Maximum Safe Operating Area	Figure 10. Single Pulse Maximum Power Dissipation

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	

Diode Recovery Test	

Package Outline

DFN5X6_P, 8leads